

**MOTOROLA**

## Dual 4-5-Input OR/NOR Gate

**ELECTRICALLY TESTED PER:  
5962-8756901**

The 10H609 is a Dual 4-5-input OR/NOR gate.

- Propagation Delay Average, 0.75 ns Typical
- 180 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

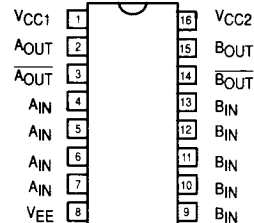
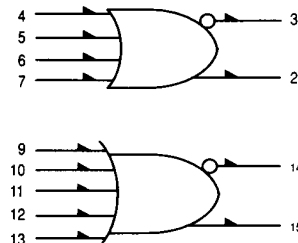
FUNCTION	PIN ASSIGNMENTS			BURN-IN (CONDITION C)
	DIL	FLATS	LCC	
VCC1	1	5	2	GND
AOUT	2	6	3	51 $\Omega$ to V <sub>TT</sub>
$\overline{AOUT}$	3	7	4	51 $\Omega$ to V <sub>TT</sub>
A <sub>1IN</sub>	4	8	5	51 $\Omega$ to V <sub>TT</sub>
A <sub>1IN</sub>	5	9	7	OPEN
A <sub>1IN</sub>	6	10	8	OPEN
A <sub>1IN</sub>	7	11	9	GND
VEE	8	12	10	VEE
B <sub>1IN</sub>	9	13	12	GND
B <sub>1IN</sub>	10	14	13	GND
B <sub>1IN</sub>	11	15	14	GND
B <sub>1IN</sub>	12	16	15	OPEN
B <sub>1IN</sub>	13	1	17	CP1
BOUT	14	2	18	51 $\Omega$ to V <sub>TT</sub>
$\overline{BOUT}$	15	3	19	51 $\Omega$ to V <sub>TT</sub>
VCC2	16	4	20	GND

**BURN - IN CONDITIONS:****V<sub>TT</sub> = - 2.0 V MAX/ - 2.2 V MIN****V<sub>EE</sub> = - 5.7 V MAX/ - 5.2 V MIN****Military 10H609****AVAILABLE AS**

- 1) JAN: N/A
  - 2) SMD: 5962-8756901
  - 3) 883: 10H609/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E  
CERFLAT: F  
LCC: 2

The letter "M" appears before  
the slash on LCC.

**LOGIC DIAGRAM**



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- The diagram illustrates the timing characteristics of a push-pull output stage. It shows five waveforms:  $V_{IN}$ ,  $PS1$ ,  $PS2$ ,  $V_{OUT}$ , and  $\overline{V_{OUT}}$ . The input  $V_{IN}$  is a square wave with rise time  $t_r$ . The push-pull transistors  $PS1$  and  $PS2$  are driven by  $V_{IN}$ . The output  $V_{OUT}$  is the voltage at the load during the high state, and  $\overline{V_{OUT}}$  is the voltage during the low state. Key timing parameters are labeled:  $t_{PHL}$  (propagation delay high-to-low),  $t_{PLH}$  (propagation delay low-to-high),  $t_{THL}$  (turn-off delay high-to-low),  $t_{TLH}$  (turn-on delay low-to-high), and  $t_r$  (rise time). The output transitions are marked at 80%, 50%, and 20% voltage levels.

MOTOROLA MILITARY MECL DATA  
2-162

# 10H609 QUIESCENT LIMIT TABLE \*

## \* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100  $\Omega$  resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V <sub>IH1</sub>	V <sub>IL1</sub>	V <sub>IH2</sub>	V <sub>IL2</sub>	PS1	PS2	VEE1	VEE2
T <sub>A</sub> = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.01	+0.31	-5.46	-4.94
T <sub>A</sub> = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94
T <sub>A</sub> = -55 °C	-0.84	-1.95	-1.16	-1.510	+0.28	+0.28	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0 V, Output Load = 100 Ω to - 2.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3												
	Functional Parameters:	Min	Max	Min	Max	Min	Max		V <sub>IH1</sub>	V <sub>IH2</sub>	V <sub>IL1</sub>	V <sub>IL2</sub>	VEE1	VEE2	VCC	P.U.T.		
V <sub>OH</sub>	High Output Voltage	- 1.01	- 0.78	- 0.86	- 0.65	- 1.06	- 0.84	V	4 - 7 9 - 13	4 - 7 9 - 13			8			1, 16	2, 3, 14, 159	
V <sub>OL</sub>	Low Output Voltage	- 1.95	- 1.58	- 1.95	- 1.565	- 1.95	- 1.61	V		4 - 7 9 - 13	4 - 7 9 - 13	4 - 7 9 - 13	8			1, 16	2, 3, 14, 15	
V <sub>OH1</sub>	High Output Voltage	- 1.01	- 0.78	- 0.86	- 0.65	- 1.06	- 0.84	V		4 - 7 9 - 13	4 - 7 9 - 13	4 - 7 9 - 13	8	8		1, 16	2, 3, 14, 15	
V <sub>OL1</sub>	Low Output Voltage	- 1.96	- 1.58	- 1.95	- 1.565	- 1.95	- 1.61	V	4 - 7 9 - 13	4 - 7 9 - 13	4 - 7 9 - 13	5 - 7 10 - 12	8	8		1, 16	2, 3, 14, 15	
I <sub>EE</sub>	Power Supply Current	- 30		- 33		- 33		mA					8			1, 16	8	
I <sub>IH</sub>	Input Current High		350		915		560	μA	4 - 7 9 - 13				8			1, 16	2, 3, 14, 15	
I <sub>IL</sub>	Input Current Low	0.5		0.3		0.5		μA		4 - 7 9 - 13			8			1, 16	2, 3, 14, 15	

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Test Temperature	Test Voltage Values (Volts)									
	V <sub>IH1</sub>	V <sub>IL1</sub>	V <sub>IH2</sub>	V <sub>IL2</sub>	PS1	PS2	VEE1	VEE2		
T <sub>A</sub> = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94		
T <sub>A</sub> = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94		
T <sub>A</sub> = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94		

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
Functional Parameters:		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to - 2.0 V, VEEL = - 2.94 V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max							
t <sub>TLH</sub>	Rise Time	0.4	1.5	0.4	1.6	0.4	1.3	ns	V <sub>IN</sub>	V <sub>OUT</sub>	V <sub>CC</sub>	V <sub>VEEL</sub>	P.U.T.	
t <sub>FHL</sub>	Fall Time	0.4	1.5	0.4	1.6	0.4	1.3	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15	
t <sub>pHL</sub>	Propagation Delay Data	0.4	1.4	0.4	1.9	0.4	1.3	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15	
t <sub>pLH</sub>	Propagation Delay Enable	0.4	1.4	0.4	1.9	0.4	1.3	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15	